









#### **Overview of Presentation**

- What is SKARAB?
- Designing/manufacturing SKARAB
- Demo of SKARAB platform





#### What is the "SKARAB"?



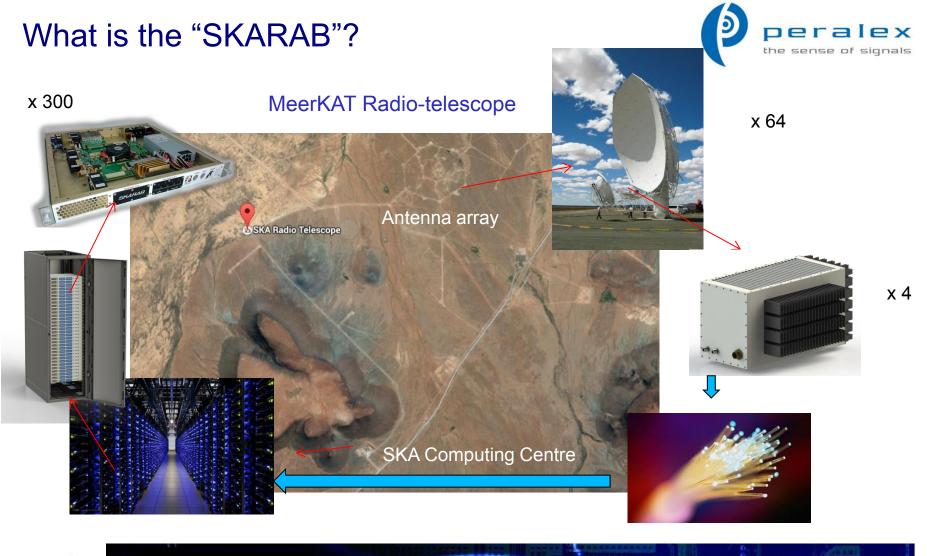
- SKARAB is an agile, extreme scale, networked, FPGA-centric cluster computing node
- SKARAB = Square Kilometre Array Reconfigurable Application Board
- SKARAB is the next generation/successor to the ROACH2 platform, conceptualised by SKA-SA
- Peralex won the tender to design and manufacture 300 SKARAB units for the MeerKAT precursor to the SKA radio-telescope in South Africa
- SKARAB is NOT application-specific!





Hello

World!

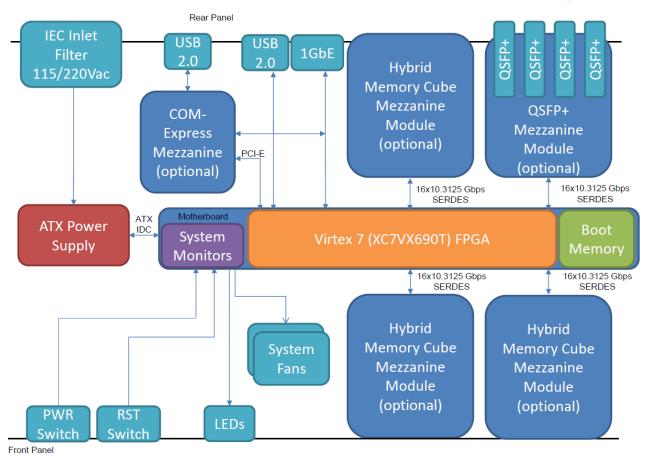






# **SKARAB Block Diagram**



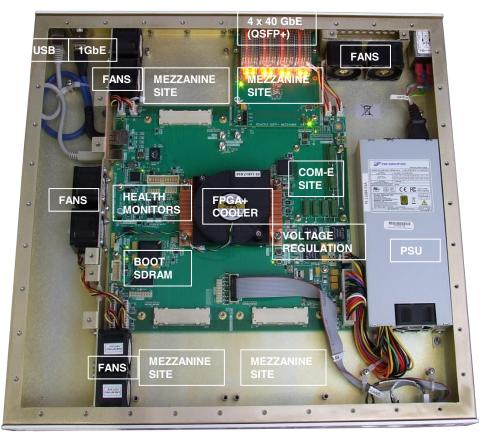






## SKARAB: Under The Hood





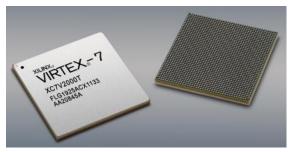




## SKARAB Compute: Virtex 7 FPGA



- 693120 Logic Cells
- 80 x SERDES
  - 64 used for I/O mezzanine sites @ 10 Gbps
  - 1 used for PCI-E to COM-E module site
- 1470 x 36Kb RAM Blocks (~52 Mb)
- 3600 DSP Slices
- 1927 pins



		Part Number	XC7VX690T				
	EasyPath™ (	Cost Reduction Solutions (1)	XCE7VX690T				
Logic		Slices	108,300				
		Logic Cells	693,120				
Resources		866,400					
Mamani	Maxim	num Distributed RAM (Kb)	10,888				
Memory	Block RAM/	1,470					
Resources		Total Block RAM (Kb)	52,920				
Clocking		20					
1/0 P	N	1/O laximum Single-Ended	1,000				
I/O Resources	Maxi						
		DSP Slices	3,600				
		_					
		PCIe Gen3	3				
Integrated IP	Analog N	Mixed Signal (AMS) / XADC	1				
Resources	Configu	1					
	GTX Transceive	_					
	GTH Transceive	80					
	GTZ Transceive	_					
		-1, -2					
Speed Grades		-2L, -3					
		-1, -2					
_	Package <sup>(6)</sup>	Dimensions (mm)	GTH)				
	FFG1157 / FFV1157 <sup>(7)</sup>	35 x 35	0, 600 (0, 20)				
Footprint	FFG1761 / FFV1761 <sup>(7)</sup>	42.5 x 42.5	0, 850 (0, 36)				
Compatible	FHG1761	45 x 45					
	FLG1925	45 x 45					
	FFG1158 / FFV1158 <sup>(7)</sup>	35 x 35	0, 350 (0, 48)				
Footprint	FFG1926	45 x 45	0, 720 (0, 64)				
Compatible	FLG1926	45 x 45					
	FFG1927 / FFV1927 <sup>(7)</sup>	45 x 45	0, 600 (0, 80)				
Footprint	FFG1928	45 x 45					
Compatible	FLG1928	45 x 45 45 x 45					
Footprint	FFG1930	0, 1000 (0, 24)					
Compatible	FLG1930	45 x 45					

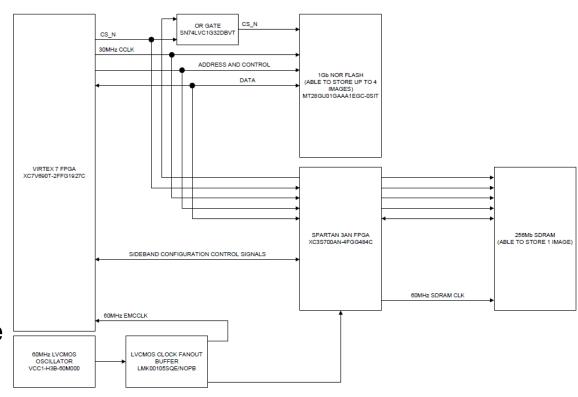




## **SKARAB: FPGA Configuration**



- Requirement to boot in under 1 second
- On power-up, FPGA boots from NV onboard boot flash (boot image and backup image)
- After power-up FPGA can be rebooted over 1GbE network interface using SDRAM-based high-speed boot mode







#### **SKARAB Mezzanine Sites**



- 400 pin FCI Megarray connector (28 Gbps capable)
- 16 x ~10 Gbps SERDES from FPGA
- 1-Wire Interface (Configuration PROM)
- Low speed I2C Management interface, PD, Fault
- JTAG interface (test)
- 12V (bulk), 5V, 3.3V
- High speed Clocks (in/out)

			PHY22_LANE1				PHY22_LANE3					PHY21_LANE1			PHY21_LANE3				PHY12_LANE1				PHY12_LANE3				PHY11_LANE1			PHY11_LANE3									
40	39	38	37	36	35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
A VCC	GND	12V	5V	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	Tm	SCL	SDA A
B VCC	GND	12V	5V	GND	RXP	GND	RXP	GND	RXP	GND	RXP	GND	RXP	GND	RXP	GND	RXP	GND	RXP	GND	RXP	GND	RXP	GND	RXP	GND	RXP	GND	RXP	GND	RXP	GND	RXP	GND	RXP	GND	AD2	TCK	TMS B
C VCC	GND	12V	5V	GND	RXN	GND	RXN	GND	RXN	GND	RXN	GND	RXN	GND	RXN	GND	RXN	GND	RXN	GND	RXN	GND	RXN	GND	RXN	GND	RXN	GND	RXN	GND	RXN	GND	RXN	GND	RXN	GND	AD1	TDO	TDI C
D VCC	GND	12V	5V	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	AD0	IRQ	1W D
E VCC	GND	12V	5V	GND	OPT	GND	OPT	GND	OPT	GND	OPT	GND	OPT	GND	OPT	GND	OPT	GND	OPT	GND	OPT	GND	OPT	GND	OPT	GND	OPT	GND	OPT	GND	OPT	GND	OPT	GND	OPT	GND	Hn	RST_N	Fn_E E
F VCC	GND	12V	5V	GND	OPT	GND	OPT	GND	OPT	GND	OPT	GND	OPT	GND	OPT	GND	OPT	GND	OPT	GND	OPT	GND	OPT	GND	OPT	GND	OPT	GND	OPT	GND	OPT	GND	OPT	GND	OPT	GND	GND	GND	GND F
G SD	GND	12V	5V	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	CKloN	CK1 <sub>0</sub> P	GND G
H Vsen•	GND	12V	5V	GND	TXP	GND	TXP	GND	TXP	GND	TXP	GND	TXP	GND	TXP	GND	TXP	GND	TXP	GND	TXP	GND	TXP	GND	TXP	GND	TXP	GND	TXP	GND	TXP	GND	TXP	GND	TXP	GND	GND	GND	GND H
J Vsen	GND	12V	5V	GND	TXN	GND	TXN	GND	TXN	GND	TXN	GND	TXN	GND	TXN	GND	TXN	GND	TXN	GND	TXN	GND	TXN	GND	TXN	GND	TXN	GND	TXN	GND	TXN	GND	TXN	GND	TXN	GND	CKIN	CKTP	GND J
K VCCm	GND	12V	5V	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND K
40	39	38	37	36	35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
				P	HYZZ_LAI	NE0		PI	HYZZ_LAN	Æ2		PI	HY21_LAN	IE0		PH	HYZ1_LAN	IE2		PH	IY12_LAN	Eθ		PI	HY1Z_LAN	(EZ		PE	IY11_LAI	IE0		PI	IY11_LAI	IEZ .					





## SKARAB Mezzanine: 4 x 40 GbE QSFP+



- Two variants (direct vs retimed)
- 4 x QSFP+ interfaces (16 x 10 Gbps)
  - Support for Copper, AOC, SR, LR fibre cables
- 32-bit ARM uC (management, PHY boot)
- Thermal sensor
- Configuration PROM
- Clock generation











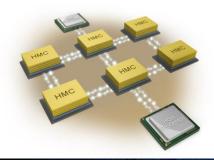
## SKARAB Mezzanine: Hybrid Memory Cube



- Mezzanine designed by SKA-SA
- 10 Gbps x 16 SERDES interface to FPGA
- 2 or 4 GB Micron HMC devices

the sense of signals

- Energy efficient (relative to DDR3/4)
- High bandwidth (relative to DDR3/4)
- Large capacity (relative to QDR SRAM/Bandwith Engine)







## **SKARAB Platform Management**



#### Consists of:

- FPGA configuration
- Autonomous/programmable fan control
- Autonomous voltage, current and fan protection/monitoring (automatic shutdown on fault)
- Blackbox recording of faults
- Diagnostic "always-on" USB interface allows access to fault logs even when unit is off.

#### Network Platform Management

- DHCP, PING available on ALL Ethernet interfaces
- Health monitoring functions available on ALL Ethernet interfaces
- High speed (<1s) FPGA configuration (through 1 GbE interface only)</li>

### Diagnostics

- USB/JTAG access to JTAG-compliant devices on motherboard and mezzanines
- Serial port interface to Microblaze processor





## **SKARAB Board Support Package**



### Consists of:

- FPGA firmware infrastructure (HDL) required for remote platform/cluster management and standard interfaces (I/O, memory)
- Windows/Linux C++ host library and executables for platform management (health monitoring, FPGA reconfiguration over LAN etc)





## SKARAB Board Support Package Firmware



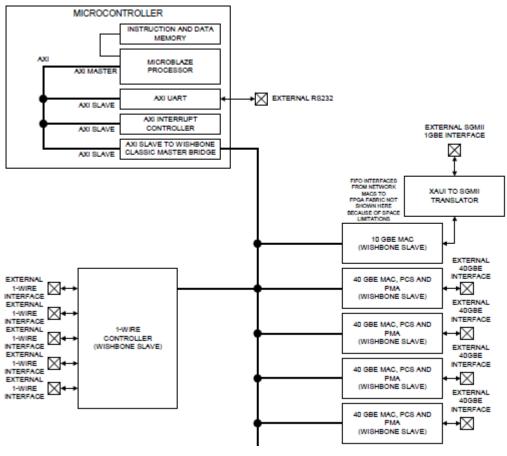
- 1 Gb Ethernet core (health monitoring, control)
  - MAC only (external PHY)
- 40 Gb Ethernet core (high speed data)
  - MAC
  - PHY (XLAUI/XLPPI to external PHY/QSFP+)
- Hybrid Memory Cube controller core (SKA-SA)
- Management microcontroller
  - MicroBlaze uC with Wishbone peripheral bus
  - 1-Wire Configuration PROM access
  - Voltage/current monitors (12 rails)
  - Fan control/status
  - High speed network-based FPGA boot
  - Network setup/management for 1 GbE and 40 GbE interfaces (PING, DHCP, etc)





# SKARAB BSP Firmware Block Diagram (1)



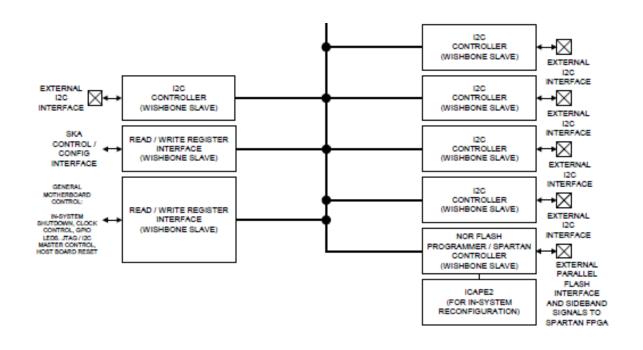






# SKARAB BSP Firmware Block Diagram (2)





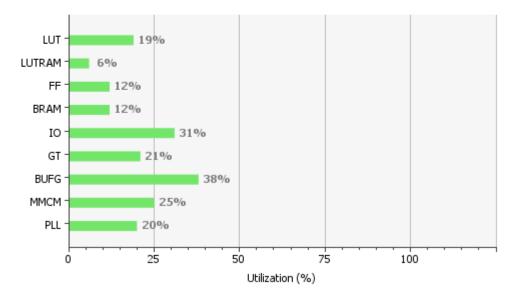


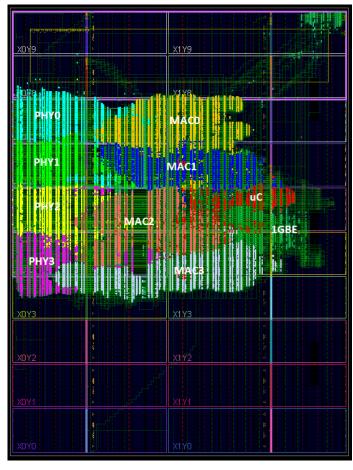


# **SKARAB Firmware Footprint**



Resource	Utilization	Available	Utilization %
LUT	81084	433200	18.72
LUTRAM	10163	174200	5.83
FF	99707	866400	11.51
BRAM	176	1470	11.97
IO	184	600	30.67
GT	17	80	21.25
BUFG	12	32	37.50
MMCM	5	20	25.00
PLL	4	20	20.00









# SKARAB: Some Interesting Platform Features



### FPGA-centric (FPGA-only!) compute platform

- Low power consumption (relative to GPU/CPU) = low operational cost ~45W (100-125W with memory)
- Reduced product complexity = simpler development (software layering/configuration management)

#### Flat architecture

- Uniform, highly scalable networked processing cluster
- · Easy adoption, "bite-size" unit scaling
- Scalable platform management
- Fault tolerance through over-provisioning/network traffic rerouting

## Configurable Memory versus I/O Bandwidth

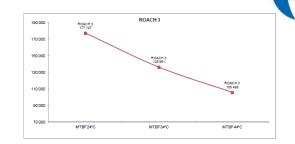
- Mezzanine tile architecture
- Semi-independent upgrade path (memory vs I/O vs compute)



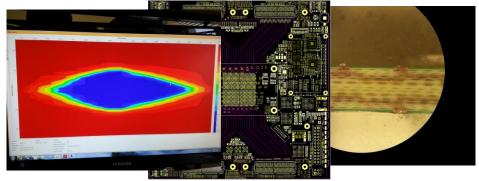


## Designing a SKARAB

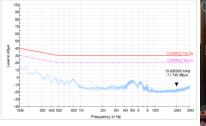
- MTBF analysis fed back into design to maximise reliability
- Thermal analysis (CFD and real-world models)
- Extensive Signal Integrity analysis and verification (IBIS-AMI, TDR, eye diagrams, BER) to meet 10.3125 Gbps over >7m on 128 links.
- Thorough environmental qualification (EMC/RFI, temperature, shock and vibration)

















## Manufacturing a SKARAB



- Internal and supply chain quality management
- PCB delamination stressing
- X-RAY/AOI of all boards
- Thermal stress screening (eliminate infant mortality)
- Automated ATP
- Optimised assembly and test harnesses.





#### Conclusion



- SKARAB hardware and BSP have been thoroughly tested (against requirements specification) and are ready for use.
- SKARAB early production units are available now. We have just moved into to volume production.
- HMC V1 HW prototypes/firmware are working on the SKARAB platform, with V2 boards currently in production.



